WHAT IS CLAIMED IS:

1. A method for amplifying an input current signal to provide an output current signal according to a predetermined gain profile, the method comprising:

providing a first and a second semiconductor device each having at least a control terminal and two current terminals for a current to flow therethrough, wherein said input current signal is fed through said current terminals of said first semiconductor device and said output current signal passes through said current terminals of said second semiconductor device;

controlling a second voltage level of said control terminal of said second semiconductor device such that said second voltage level follows a first voltage level of a control terminal of said first semiconductor device;

providing circuitry responsive to said input current signal to provide said first voltage level such that said first voltage level varies with said input current signal to cause said second semiconductor device to generate said output current signal according to said predetermined gain profile, wherein said circuitry biases said first semiconductor device in a first operating region, and wherein said second semiconductor device is biased in a second operating region having a higher device-current to control-voltage ratio than said first operating region.

2. A method as claimed in claim 1, wherein said circuitry biases said first semiconductor device in a triode region.

3. A method as claimed in claim 2, wherein said circuitry

biases said second semiconductor device in a saturation region.

4. A method as claimed in claim 1, wherein said providing circuitry comprises providing a third semiconductor device having at least a control terminal and two current terminals for a current to flow therethrough, said third semiconductor device connected to said first semiconductor device in such a way that said control terminal of said third semiconductor device can adjust a voltage across said current terminals of said first semiconductor device, while a signal at said control terminal of said first semiconductor device still varies according to said input current signal.

5. A method as claimed in claim 1, wherein said predetermined gain profile is adaptive, and said providing circuitry comprises providing a feedback system which causes a voltage across said current terminals of said first semiconductor device to vary as a function of said input current signal such that a decrease of said input current signal will produce a sufficient change in said voltage across said current terminals to result in an increase in current gain.

6. A method as claimed in claim 5, wherein said providing circuitry comprises providing a third semiconductor device having at least a control terminal and two current terminals for a current to flow therethrough, said third semiconductor device connected to said first semiconductor device in such a way that said control terminal of said third semiconductor device can adjust said voltage across said current terminals of said first device, while a signal at said control terminal

of said first semiconductor device still varies according to said input current signal.

7. A method as claimed in claim 6, wherein said providing a feedback system comprises feeding back said first voltage level of said first semiconductor device to said control terminal of said third semiconductor device such that a decrease in said first voltage level will result in a lower voltage at said control terminal of said third semiconductor device.

8. A method as claimed in claim 7, wherein said feeding back said first voltage level comprises feeding back via a voltage divider, wherein a division ratio is controlled by said first voltage level.

9. A method as claimed in claim 8, wherein said voltage divider comprises a pair of semiconductor devices cascoded together between an upper supply voltage and a lower supply voltage.

10. A circuit for amplifying an input current signal to provide an output current signal according to a predetermined gain profile, the circuit comprising:

a first semiconductor device having at least a control terminal and two current terminals for a current to flow therethrough, wherein said input current signal passes through said current terminals of said first semiconductor device;

a second semiconductor device having at least a control terminal and two current terminals for a current to flow therethrough, wherein a second voltage level of said control

terminal of said second semiconductor device follows a first voltage level of said control terminal of said first semiconductor device, and wherein said output current signal passes through said current terminals of said second semiconductor device; and

circuitry responsive to said input current signal to provide said first voltage level such that said first voltage level varies with said input current signal to cause said second semiconductor device to generate said output current signal according to said predetermined gain profile, wherein said circuitry biases said first semiconductor device in a first operating region, and wherein said second semiconductor device is biased in a second operating region having a higher device-current to control-voltage ratio than said first operating region.

11. A circuit as claimed in claim 10, wherein said first semiconductor device is biased in a triode region by said circuitry.

12. A circuit as claimed in claim 11, wherein said second semiconductor device is biased in a saturation region by said circuitry.

13. A circuit as claimed in claim 10, wherein said circuitry comprises a third semiconductor device having at least a control terminal and two current terminals for a current to flow therethrough, in series with said first semiconductor device such that said input current signal is fed through said current terminals of said third semiconductor device, and wherein said input current terminal of said third

semiconductor device is connected to said control terminal of said first semiconductor device, whereby applying a control signal to said control terminal of said third semiconductor device sets a voltage across said first semiconductor device.

14. A circuit as claimed in claim 10, wherein said first semiconductor device and said second semiconductor device are metal-oxide field effect transistors.

15. A circuit as claimed in claim 14, wherein said first semiconductor device and said second semiconductor device have substantially identical size aspect ratios.

16. A circuit as claimed in claim 10, wherein said predetermined gain profile is adaptive, and said circuitry comprises a feedback system which causes a voltage across said current terminals of said first semiconductor device to vary as a function of said input current signal such that a decrease of said input current signal will produce a sufficient change in said voltage across said current terminals of said first semiconductor device to result in an increase in current gain.

17. A circuit as claimed in claim 16, wherein said circuitry comprises a third semiconductor device having at least a control terminal and two current terminals for a current to flow therethrough, in series with said first semiconductor device such that said input current signal is fed through said current terminals of said third semiconductor device, and wherein one of said current terminals of said third semiconductor device is connected to said control terminal of

said first semiconductor device, whereby applying a control signal to said control terminal of said third semiconductor device sets said voltage across said first semiconductor device.

18. A circuit as claimed in claim 17, wherein said feedback system comprises a voltage divider between said control terminal of said first semiconductor device and said control terminal of said third semiconductor device, wherein a division ratio is controlled by said first voltage level.

19. A circuit as claimed in claim 18, wherein said voltage divider comprises a pair of semiconductor devices cascoded together between an upper supply voltage and a lower supply voltage.